INTERNAL CACHE FOR ON CHIP TEST DATA STORAGE

ABSTRACT

A method of testing a semiconductor device having a memory is disclosed. The method includes selecting a portion of the memory; testing the selected portion of the memory; designating the selected portion of the memory as a designated memory in response to an acceptable testing result; and storing data in the designated portion of the memory for retrieval at a later time. Provision for soft repair of the selected memory is made. Test data can be compressed before being stored in the designated memory.